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| Document Name | | | | | | | | | | | | | | | | | | Document Number  00.06.01.405 | | | | | | | |
| Ford FPD Link Implementation Review Checklist | | | | | | | | | | | | | | | | | |  | | | | | | | |
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| DATE | | |  | |  | REVISIONS | | | | | | | | | | | | |  | |  | REFERENCE | | | |
| 6/22/2018 | | |  | | AA | Initial Release | | | | | | | | | | | | |  | |  |  | | | |
| 3/21/2018 | | |  | | AB | Added requirement 3.1.2.2 and 3.3.1.8, Updated requirement numbers | | | | | | | | | | | | |  | |  | MODIFIED BY | | | |
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# INTRODUCTION

## 1.1 Purpose

This Implementation Review Checklist document may be used to evaluate and/or certify the conformance of Ford FPD LINK vehicle networks.

Any network implementation that passes all checklist entries specified herein shall be considered “production ready”.

## 1.2 Scope

This DV plan identifies the required tests required to be performed to verify a module that incorporates FPD LINK meets the Ford FPD LINK requirements

## 1.3 Use of this Document

This document provides a formal test procedure to evaluate the integrity of Ford FPD LINK based vehicle system networks. Systems and subsystem integrators must perform the tests within this document as deemed within the program specific "Statement Of Work”. The tests within may be applied to any system implementation that has been designed in accordance to the Ford FPD LINK specifications identified in section 1.4 of this document. The individual test cases contained in this document may be performed in any sequence, subset, or performed repetitively, for the purposes of troubleshooting and/or evaluation. For vehicle program "Engineering Sign-Off Certification" however, all tests must be performed sequentially, in full, and have a formal TDR completed and provided to their respective Ford Mux Applications Engineering Authority. In addition, all delineations and options within this document must be identified and adhered to

## 1.4 Ford Documentation References

The requirements of the document listed in the following table form a part of this specification. The revision levels shown in the the table were the latest at the time this Functional Specification was written. In the event of a conflict between the requirements of this specification and these documents in the table shall have precedence

| **Rev Level** | **Requirement Document Name (ie, SDS/ARL requirements, Deviations, Engineering Specifications)** |
| --- | --- |
|  | [1] - FPD LINK Physical Layer Specification 00.06.03.004 |
|  | [2] - Netcom Physical Layer Approved Components 00.06.03.002 |
|  | [3] - Feature – I2C over LVDS Communication Protocol [VDOC038838] |
|  | [4] - Texas Instruments Data sheets and user guides |
|  | [5] - FPD Link Physical Layer Design Verification Checklist 00.06.03.401 |
|  | [6] - FPD Link Implementation Specification 00.06.01.004 |
|  | [7] – TI datasheets1 |
|  | [8] – FPD LINK Cable/Connector Assembly Specification 00.06.01.005 |

**Table (1) Document References**

## 1.5 Definitions/Abbreviations

### 1.5.1 General Definitions

|  |  |
| --- | --- |
| Back Channel | Low speed data channel over which command and control data is sent |
| Bus | A bus is a collection of one or more wires connecting two or more nodes. Each electronic device (in this case: Host ECU, Master Node or Slave Node) is equipped with a specific, standardised electronic interface in order to guarantee compatibility between exchanged binary items of information |
| Deserializer | The deserializer converts FPD LINK frames raw into video/display data |
| Display Processor | This is video data sink typically on the head unit or cluster or display module. It is connected to an FPD LINK Deserializer via I2C and high speed data lines. |
| Forward Channel | High speed data channel over which raw/uncompressed video data is sent |
| Host ECU | Electronic control unit that communicates on the CAN Network that uses FPD LINK to send and receive data to peripheral devices |
| Host Microprocessor | Microprocessor unit that is part of the Host ECU that interfaces with the local node |
| Local Node | Local Node is attached to the main system processor and is responsible configuration and PowerModing of the bus |
| Multiplex | To interleave or simultaneously transmit two or more messages/signals or sets of data on a single channel. |
| Network | A set of electronic and cabling devices facilitating the multidirectional exchange of information between two or more nodes on one or more busses. |
| Remote Node | Remote Node is attached to the Local node via FPD LINK and it receives it’s configuration and Powermoding from the local node over FPD LINK |
| Sensor | This is a data source like camera imager, lidar sensor etc. It is connected to an FPD LINK Serializer via I2C and high speed data lines. The sensor can be configured from FPD LINK from the back channel data. |
| Serializer | The serializer converts raw video/display data into FPD LINK frames and sends this over the data line at high bit rates |
| Pixel Clock | Product of image resolution frame rate colour depth and blanking interval |
| REF Clock | Driving FPD link when operating in sync mode |
| CSI-2 clock | Determines CSI data rate per lane |
| Ext clock mode | Clock driving serilizer independent of deserializer clock |
| DVP clock | Special case of external clock for backward compatibility |
| Sync mode | Using single REF clock to drive both serializer and deserializer |
| CMLOUT | FPD link without backchannel used in dasy chain |

Table (2) Requirement Documents

### 1.5.2 Abbreviations used in this document

|  |  |
| --- | --- |
| BCC | Bi-Directional Control Channel |
| DID | Diagnostic Identifiers |
| DTC | Diagnostic Trouble Code |
| ECU | Electronic Control Unit |
| EMC | Electromagnetic Compatibility |
| FMC | Ford Motor Company |
| FPD LINK | Flat Panel Display (FPD) Link III (TI Devices Trademark) |
| FPS | Frames Per Second |
| DL | High Level Hardware and Software Link |
| ISO | International Standards Organisation |
| LVDS | Low Voltage Differential Signalling |
| PCB | Printed Circuit Board |
| PDB | Power Down Mode Pin |
| POC | Power Over Coax |
| PoDL | Power over Data Line (same as in POC) |
| SERDES | Serializer-Deserializer |
| TI | Texas Instruments |
| STP | Shielded Twisted Pair |
|  |  |
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|  |  |
| --- | --- |
| BCC | Bi-Directional Control Channel |
| DID | Diagnostic Identifiers |
| DTC | Diagnostic Trouble Code |
| ECU | Electronic Control Unit |
| EMC | Electromagnetic Compatibility |
| FMC | Ford Motor Company |
| FPD LINK | Flat Panel Display (FPD) Link (TI Devices Trademark) |
| FPS | Frames Per Second |
| ISO | International Standards Organisation |
| LVDS | Low Voltage Differential Signalling |
| PCB | Printed Circuit Board |
| PDB | Power Down Mode Pin |
| POC | Power Over Coax |
| PoDL | Power over Data Line (same as in POC) |
| SERDES | Serializer-Deserializer |
| TI | Texas Instruments |
| STP | Shielded Twisted Pair |
| CMLOUT | Current mode logic output |

Table (3) Abbreviations

# Design Verification Checklist

## 2.1 FPD LINK Node Conformance Tests

All FPD LINK Nodes must demonstrate conformance to the applicable tests defined in the table below:

| **FPD LINK Checklist Items** | **Checklist items Evidence** | **Pass/ Fail/Comments** |
| --- | --- | --- |
| **Maximum Clock Rate**  DL\_FPD LINK\_REQ\_\_3.1.1.1  Is the clock sufficient for the image properties: Frame rate, Resolution, Bit depth and overhead.  Show the calculations.    Confirm the chipsets maximum video rate, Maximum pixel clock, CSI-2 Rate meets requirements [Ref(1)] and the corresponding data sheet |  |  |
| **Forward Channel Data Rate**  DL\_FPD LINK\_REQ\_\_3.1.2.1  DL\_FPD LINK III\_LINK\_REQ\_\_3.1.2.2  Show the calculations and prove the chosen chipsets meets the forward channel data rate  Confirm the chipsets forward channel data rate and corresponding frequency range meets requirements [Ref(1)] and the corresponding data sheet  Confirm the use of appropriate cable/connectors assemblies for the corresponding channel frequency range for forward channel. |  |  |
| **Back Channel Data Rate**  DL\_FPD LINK\_REQ\_\_3.1.3.1  Is the back channel bandwidth sufficient for the amount of data needs to be transported between remote node to local node  What is expected data. Show the calculations    Confirm the chipsets back channel data rate and correspondinh frequency range meets requirements [Ref(1)] and the corresponding data sheet  Confirm the use of appropriate cable/connectors assemblies for the corresponding channel frequency range for back channel. |  |  |
| **Supported Formats**  DL\_FPD LINK\_REQ\_\_3.1.4.1  Confirm the supported chipsets Video format provided to serializer, CSI data type on Deserializer meets the requirements [Ref(1)] |  |  |

**Table (4)**

## 2.2 FPD LINK Local Node Conformance Tests

If the ECU is local node, Perform the review below. If ECU is remode node, perform review in 2.3

|  |  |  |
| --- | --- | --- |
| **FPD LINK Checklist items** | **Checklist items Evidence** | **Pass/ Fail/ Comments** |
| **Common FPD LINK Network Wakeup Source**  DL\_FPD LINK\_REQ\_\_3.2.3.1  What is the source of the local node wakeup?  What is the method/feature used by the source to supply power to remote node?  Any deviations should be reviewed and approved by Advance Netcom team |  |  |
| **Local Node Initialization**  DL\_FPD LINK\_REQ\_\_3.3.1.1  Confirm that the local node initializes the chipsets registers of both local and remote node by the Host ECU  Confirm the chipset registers intialized meets the requirements of the Local node setup, I2C remote communication configuration, Link status check [Ref(1)] |  |  |
| **Chipset Power- Up**  DL\_FPD LINK\_REQ\_\_3.3.1.2  Confirm the chipset Power-Up sequencing and PDB Pin setup comply with the requirements [Ref(1)] and datasheets  Show the evidence as simulation results and/or scope plots |  |  |
| **Intialization time**  DL\_FPD LINK\_REQ\_\_3.3.1.3  Confirm the Intialization time of the FPD LINK network meets the requirements [Ref(1)]  Show the evidence as simulation results and/or scope plots |  |  |
| **Video Master Clock**  DL\_FPD LINK\_REQ\_\_3.3.1.4  Confirm the supply of Video Master Clock of the FPD LINK network meets the requirements [Ref(1)]  Show the evidence as simulation results and/or scope plots |  |  |
| **Software Drivers**  DL\_FPD LINK\_REQ\_\_3.3.1.5  Confirm the usage of the approved FPD LINK software driver meets the requirements [Ref(1)]  Confirm the driver supports I2C communication with the local host, status monitoring, interrupts, diagnostics and error recovery |  |  |
| **GPIO state during loss of lock**  DL\_FPD LINK\_REQ\_\_3.3.1.7  Confirm No GPIO pins are driven during a loss of lock event  Show the evidence as simulation results and/or scope plots |  |  |
| **Disabling unused channels on hubs**  DL\_FPD LINK\_REQ\_\_3.3.1.8  Confirm any unused channel in multi port chipset is disabled  Confirm how is it disabled? |  |  |
| **Loss of lock fault**  DL\_FPD LINK\_REQ\_\_3.3.2.2  Confirm the lock status between local node and remote node by reading registers  How is lock status monitored? (Hardware pin or Software register)  Confirm the loss of lock events meets the requirements [Ref(1)] by reviewing the simulation results and/or scope plots |  |  |
| **Error Detection and Reporting**  DL\_FPD LINK\_REQ\_\_3.3.2.3  Confirm the local node supports the following errors and sets the related DTC’s   1. Errors during local node FPD LINK Network Configuration 2. Hard Network Errors 3. Transient Errors |  |  |
| **Local Node Error Handling Procedure**  DL\_FPD LINK\_REQ\_\_3.3.3.1  Confirm the following strategies are used in handling the detected errors   1. Diagnostic Command Response code 2. Diagnostic DTC and related DID 3. Soft reset |  |  |
| **Remote node being unresponsive/offline**  DL\_FPD LINK\_REQ\_\_3.3.3.2  What registers confirms the fault condition of the Remote node  How is the Remote node fault condition recovered?  Show the evidence of software that handles the loss of communication with the remode node |  |  |
| **FPD LINK DTC reporting**  DL\_FPD LINK\_REQ\_\_3.4.3.1  DL\_FPD LINK\_REQ\_\_3.4.3.2  DL\_FPD LINK\_REQ\_\_3.4.3.3  DL\_FPD LINK\_REQ\_\_3.4.3.4  DL\_FPD LINK\_REQ\_\_3.4.3.5  Confirm the detection and reporting of the faults by setting the following fault DID’s, DTC’s and meets the requirements of the minimum loss of events [Ref(1)]   1. LVDS Link Fault 2. Loss of Lock 3. DID Unexpected Reset 4. DTC Reset Request 5. DTC LostComm   Show the evidence in the software code review |  |  |

**Table (5)**

## 2.3 FPD LINK Remote Node Conformance Tests

|  |  |  |
| --- | --- | --- |
| **FPD LINK Requirements** | **Requirements Evidence** | **Pass/ Fail/Comments** |
| **Remote Node Initialization**  DL\_FPD LINK\_REQ\_\_3.5.1.1  Confirm the Remote node initialization by the register values as in the requirement [Ref(1)]  Show the evidence from the software review  Confirm the register values matches between local and remote nodes |  |  |
| **Remote Node Peripheral Error Reporting and Status**  DL\_FPD LINK\_REQ\_\_3.5.2.1  DL\_FPD LINK\_REQ\_\_3.5.2.2  Confirm the counters, errors detected, reported and from the register values as in the requirement [Ref(1)]  Confirm that remote node does not report peripheral errors using the FPD LINK Network Error DTC  Confirm that a unique DTC is defined for the peripheral errors  Show the evidence from the software review |  |  |
| **Remote Node Error recovery**  DL\_FPD LINK\_REQ\_\_3.5.3.1  Confirm that the local node handles link monitoring status and error recovery on behalf of remote node  Show the evidence from the software review |  |  |

**Table (6)**

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# 3 Change Log

Record all changes made to this document in table (7)

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**Table (7)**